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(71) Applicant(s)
NEC Technologies (UK) Ltd
(Incorporated in the United Kingdom)
Castle Farm Campus, Priorslee, TELFORD, Shrops,
TF2 9SA, United Kingdom

(72) Inventor(s)
David Andrew Wheeler

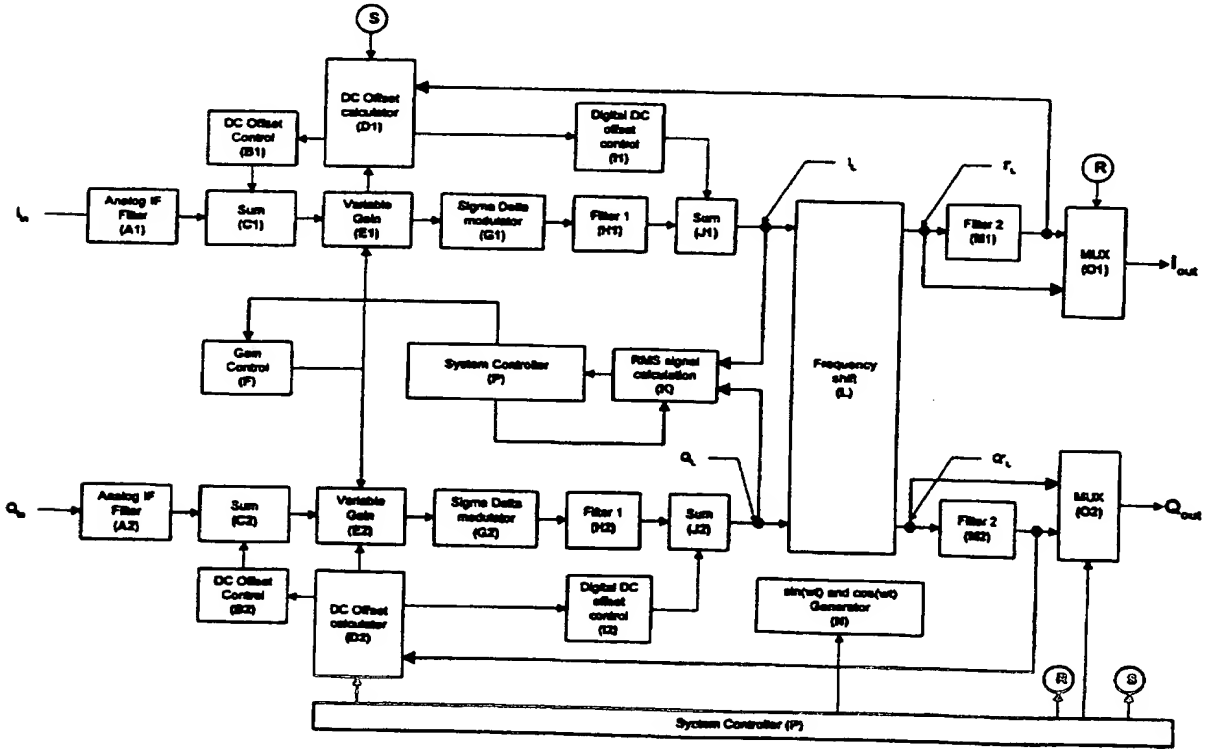
(74) Agent and/or Address for Service
Marks & Clerk
Alpha Tower, Suffolk Street Queensway,
BIRMINGHAM, B1 1TT, United Kingdom

(54) Abstract Title

GSM mobile receiver

(57) A baseband receiver arrangement for a GSM phone includes two channels for the in-phase I_{in} and quadrature Q_{in} components of the receiver signal. Each channel includes a sigma-delta modulator G1,G2 providing a high frequency single bit output data stream. There is a two stage decimation filter with the first stage H1,H2 providing a multi-bit output at a multiple of the symbol rate and the second stage M1,M2 further processing the output of the first stage to provide a multi-bit output at the symbol rate. Between the two filter stages, various other processing, such as digital frequency shifting, may be effected and dc offset correction and gain control may also be carried out on the basis of the output of the first stage filter.

The Sigma-delta modulators and the two digital filter sections form a two channel ADC.



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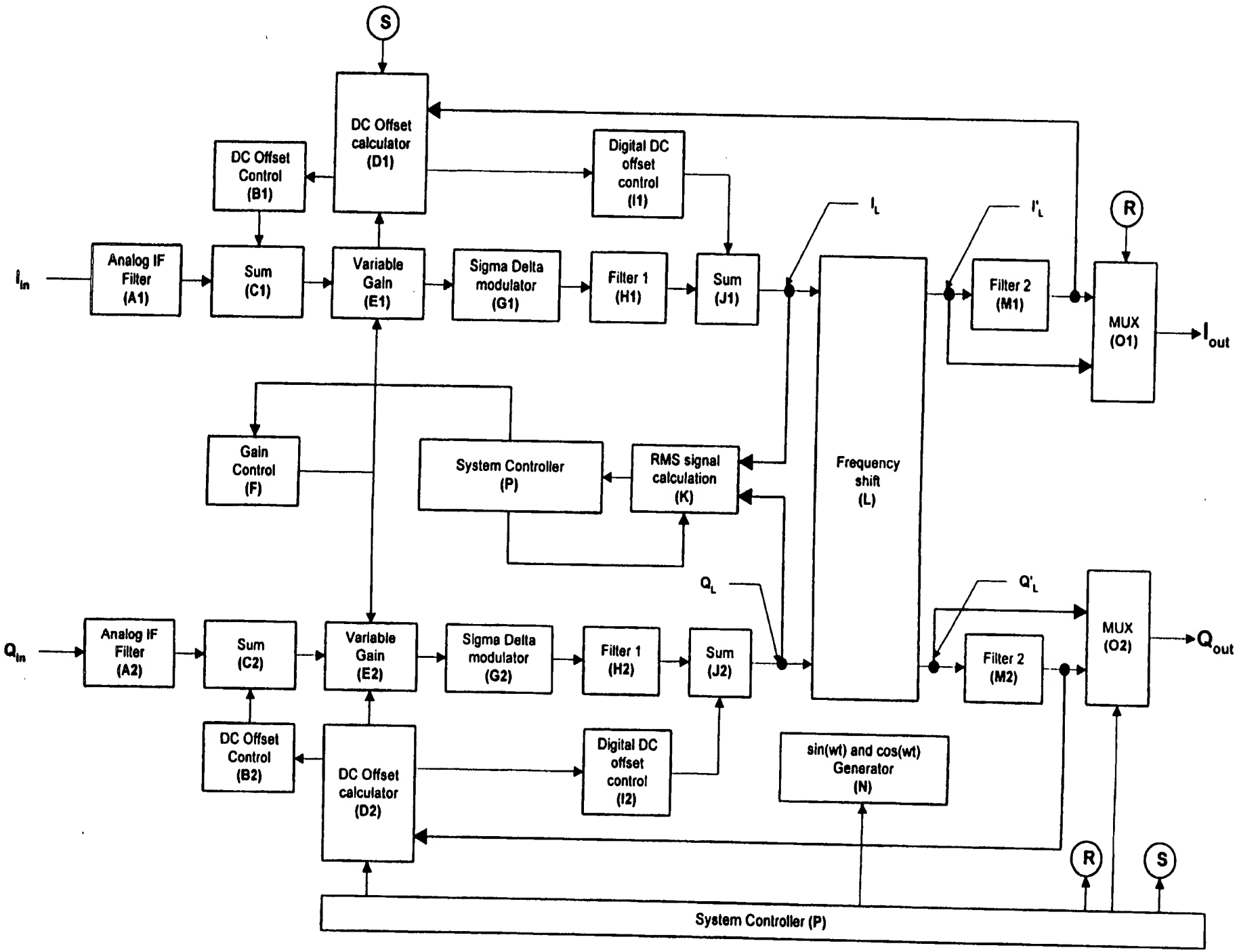

GSM MOBILE RECEIVER

This invention relates to a GSM mobile receiver and has particular reference to the GSM baseband receive architecture of the receiver.

It is an object of the present invention to provide a baseband receiver arrangement for a GSM mobile phone, in which the various baseband functions can be achieved efficiently utilising as much digital signal processing as possible.

Broadly, the invention resides in a baseband receiver arrangement for a GSM phone comprising in each of two channels for inphase and quadrature components of the received signals, a Sigma-Delta modulator for providing a high frequency single-bit data stream, a first digital filter for converting such data stream to a multi-bit signal at a multiple of the symbol rate, and a second digital filter for converting such multi-bit signal to a multi-bit output signal at the symbol rate.

Preferably, frequency correction is obtained using a complex digital frequency shifter arranged between the first and second digital filters.

Preferably dc offset cancellation is obtained by means of a coarse analog dc offset cancellation section in each channel and a digital dc offset cancellation section operating on the output of the first digital filter of each channel to provide two-stage dc offset cancellation.

Preferably, a digitally controlled analog gain control section is provided in each channel controlled by an RMS signal level calculator deriving its inputs from the output of the first digital filters.

An example of the invention is shown in the accompanying drawing of which the single figure is a block diagram of a GSM baseband receiver arrangement.

The baseband receiver arrangement shown comprises two channel for in-phase (I_{in}) and quadrature (Q_{in}) components of the received signal from an RF stage (not shown). From input to output, each channel comprises an analog IF filter section (A1, A2), an analog summing section (C1, C2) used for coarse dc offset cancellation, a variable gain section (E1, E2), a Sigma Delta modulator (G1, G2), a first digital filter state (H1, H2) and a digital summing section (J1, J2) used for fine dc offset cancellation, a frequency shifter (L), which is common to both channels, a second digital filter stage (M1, M2) and a multiplexer (O1, O2) which can selective pass to the outputs the output of the second filter stage or that of the frequency shifter L.

The analog IF filter sections A1 and A2 are third order Butterworth continuous time filters with a worst case half power point at 105KHz. Group delay ripple of these filters should be of the order of $\pm 0.5\mu S$, where the symbol period is $3.69\mu S$ (for GSM). The IF filter sections remove some of the energy in GSM channels adjacent the frequency channel to be received.

The analog variable gain sections E1, E2 are designed to amplify the signals passed by the filters A1, A2 by up to 16dB. The gain is digitally controlled in four 4dB steps so as to ensure that the dynamic range of the ADCs formed by the Sigma-Delta modulators G1, G2 and the two digital filter sections is efficiently used.

As mentioned above the Sigma-Delta modulators and the two digital filter sections form a two channel ADC. The modulators G1 and G2 operate at a sample rate of 13MHz i.e. 48 times the symbol rate. A single bit digital output stream is produced. The first digital filter sections H1 and H2 are implemented as $\{\sin(x)/x\}^3$ filters which reduce the sample rate by a factor of 16 to give a rate 3 times the symbol rate and provide a 13 bit output. The half power points of filters H1 and H2 occur at approximately 210KHz. The second digital filter sections are implemented as FIR filters with 36 taps. Each has real coefficients and linear phase which means that it can be implemented using 18 multiply accumulates. Each filter has a half power point at 95KHz and stopband rejection of 55dB from 135KHz to 406.25KHz. The filter ripple passband is less than $\pm$0.1dB.

The frequency shifter L is provided to enable the mobile station and the basestation frequency references to be synchronised. In practice frequency shifts of up to 20KHz may be required and since the samples on which the shifter L operates are at a rate three times the symbol rate large but accurate shifts are possible.

The frequency shifter operates in accordance with the following:

$$I'L = IL * C(i+f) - QL * S(i+f)$$

$$Q'L = IL * S(i+f) + QL * C(i+f)$$

where i is an integer index into a cosine table and f is a fractional interpolation value. The notation C(i+f) and S(i+f) indicate approximate cosine and sine values from a quantised table with linear interpolation. This requires 4 multiply accumulates at the 3x symbol rate equal to 12 multiply accumulates at the symbol rate. Interpolation is effected as

follows assuming for simplicity that a full cycle table of N entries is available:

$$C(i+f) = C(i) *f* \{C(i+1) - C(i)\}$$
$$S(i+f) = S(i) *f* \{S(i+1) - S(i)\}$$

$$C(i) = \cos(2\pi i/N)$$
$$S(i) = \sin(2\pi i/N)$$

DC offset cancellation is carried out in two stages using the analog summing sections C1 and C2 at the inputs to the variable gain sections E1 and E2 and the digital summing sections J1 and J2 at the inputs of the frequency shifter L.

The analog summing sections C1 and C2 receive analog offset signals from controls B1 and B2. Similarly the digital summing sections receive digital offset signals from controls I1 and I2. Both analog controls B1 and B2 and digital controls I1 and I2 are in turn controlled by DC offset calculators D1 and D2 which receive digital inputs from the respective second filter states M1 and M2.

When the mobile station is receiving on its paging channel, the DC offset calculation need be performed only once. The result read by the system controller P can be re-applied to each received burst. This can be done because the paging channel does not frequency hop and reception is so infrequent that averaging in the AGC has no effect, so the AGC might as well be held constant. In this situation the DC offset presented by the RF device will not change for burst receive. The DC offset should be re-estimated every time the AGC is changed or the receive frequency changes.

The DC offset is calculated prior to receiving a burst. The frequency offset N is set to zero for this calculation. The variable gain sections E1 and E2 are set to the values which will be used for the burst receive. The RF front end is presented to an equivalent resistance to the antenna. The calibration begins with the ADC converting 64 samples. The DC offset in each channel is estimated by accumulating samples from the second filter stages M1 and M2 and dividing the sum by 64. The result is then divided by the variable gain and negated and applied to the analog DC offset controls B1 and B2. The calibration is then continued with controls B1 and B2 applying the coarse correction just determined and the ADC converts the next 64 samples.

The DC offset of each channel is separately estimated by accumulating samples from the outputs of the second filter stages M1 and M2 and dividing the result by 64. The result is then negated and applied to the digital DC offset controls I1 and I2. This two stage process ensures that the majority DC offset that would affect the ADC dynamic range is removed prior to variable gain, and the residual DC offset is removed before digital frequency shifting. Applying DC offset correction before the digital frequency shifting ensures that DC is annulled for any subsequent shift.

The analog DC offset controls B1 and B2 are implemented as 4 bit DACs to allow the DC correction to be held indefinitely until the next calibration. The digital DC offset controls I1 and I2 are simply read/write registers to hold the calculated values.

Both variable gain sections E1 and E2 are controlled by a common gain control F. RMS signal level is calculated from the outputs of the digital

summing sections J1 and J2, i.e. the signals used are DC corrected signals which have been subjected to the first stage of digital filtration. At this stage, the 3rd adjacent channels and beyond have all been attenuated by more than 20dB, so that the RMS calculation includes only two adjacent channels on either side of the wanted channel. The RMS value is calculated as:

$$\text{sqrt (average output } (H2)^2 + \text{output}(H1)^2))$$

over a whole burst receive or by the approximation (which is easier to calculate):

$$\text{average (abs(output}(H2) + \text{output}(H1)))$$

The accumulation takes place at three times the symbol rate so that 450 samples could be used during a burst receive.

The arrangement described above provides all the required functions for the GSM baseband receiver in a very cost effective design. In particular, it should be noted that frequency correction is achieved without the need for an expensive voltage controlled crystal oscillator.

CLAIMS

1. A baseband receiver arrangement for a GSM phone comprising in each of two channels for inphase and quadrature components of the received signals, a Sigma-Delta modulator for providing a high frequency single-bit data stream, a first digital filter for converting such data stream to a multi-bit signal at a multiple of the symbol rate, and a second digital filter for converting such multi-bit signal to a multi-bit output signal at the symbol rate.

2. A baseband receiver arrangement as claimed in Claim 1, in which the sigma-delta modulators operate at 13MHz.

3. A baseband receiver arrangement as claimed in Claim 1 or Claim 2, in which said first filter stage in each channel comprises a $\{\sin(x)/(x)\}^3$ filter having a half power point at approximate 210 MHz and providing an output at three times the symbol rate.

4. A baseband receive arrangement as claimed in any preceding claim, in which the second filter stage in each channel is a FIR filter of 36 taps with a half power point of 95KHz.

5. A baseband receiver arrangement as claimed in any preceding claim, in which there is further provided a complex digital frequency shifter operating on the signals from the two channels and occurring between the first and second digital filter stages.

6. A baseband receiver arrangement as claimed in any preceding claim, further comprising a split dc offset cancellation arrangement comprising a coarse analog dc offset cancellation section in each channel and a digital dc offset cancellation section in each channel operating on the output of the first digital filter stage.

7. A baseband receiver arrangement as claimed in Claim 6, in which the two dc offset cancellation sections in each channel are controlled by a DC offset calculator which derives input samples from the output of the second digital filter stage of each channel.

8. A baseband receiver arrangement as claimed in any preceding claim, in which a digitally controlled analog gain control circuit is provided in each channel controlled by a common RMS signal level calculator deriving its inputs from the output of the first digital filter stages.

9. A baseband receiver arrangement for a GSM phone substantially as hereinbefore described with reference to the sole figure of the accompanying drawings.

The Patent Office

9

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Claims searched: 1-9 **Date of search:** 31 October 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4P PAQ H3H HAH

Int Cl (Ed.6): H03H 17/06 H03M 3/00,3/02 H04L 27/38

Other: ONLINE:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2215945 A	(STC) See, for example, figures 1 and 2 and description on page 4, last four lines to page 5 line 6.	1 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.